

L8: (79)7 with 4
L8: (79)8 with 5
L10: (49) trench
L11: (86948) trench
L12: (1614976) capacit\$4
L13: (2) 12 near 10
L14: (8637) 12 near2 11
L15: (8) 14 and 8
L18: (2) "2002118255"
L17: (261) (finfet fin adj2 (fet mosfet mos transistor))
L18: (10) 17 and 14
L19: (10) 18 and 12
L20: (132188) fin
L21: (10) 19 and 20
L22: (89493) (wordline "WL" ((word digit control adj gate) adj line) \word near (read\$
L23: (28073) 5 near9 22
L24: (8) 21 and 23
L25: (102356) (bl bitline bit adj line readline read adj line sense adj line)
L26: (6) 24 and 25
L27: (545653) (FOX field adj oxide STI (isolati\$3 (element adj (insulat\$4 separat\$
L28: (6) 26 and 27
L28: (4) ("6316813" "5567862") .pn.
L30: (195984) strap\$4
L31: (3) 29 and 30

Failed

 Saved
































#	Inventor	Document#	Issue #	Title	Current	Current XN	Retrieval	S	C	P	3	3	3	3	Image Doc	P
1	Kondo, Masa	US 20040015	2004003	Double-gate structure fin-type transistor	257/623										US 20040015	2004003
2	Brown, Jeffr	US 20040012	2004001	DRAM cell with enhanced SER immunity	438/257										US 20040012	2004001
3	Brown, Jeffr	US 20040003	2004001	DRAM cell with enhanced SER immunity	257/298										US 20040003	2004001

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